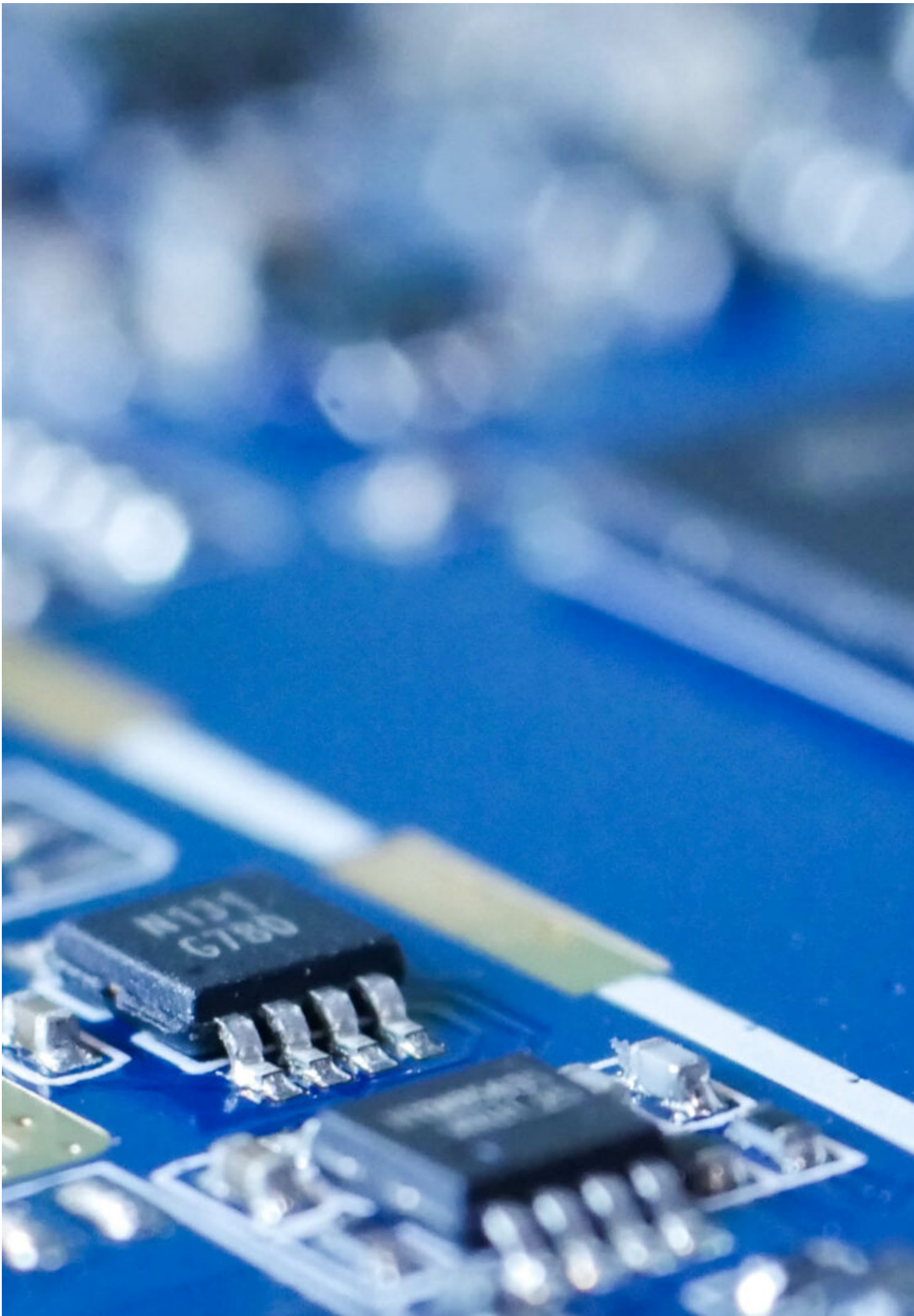
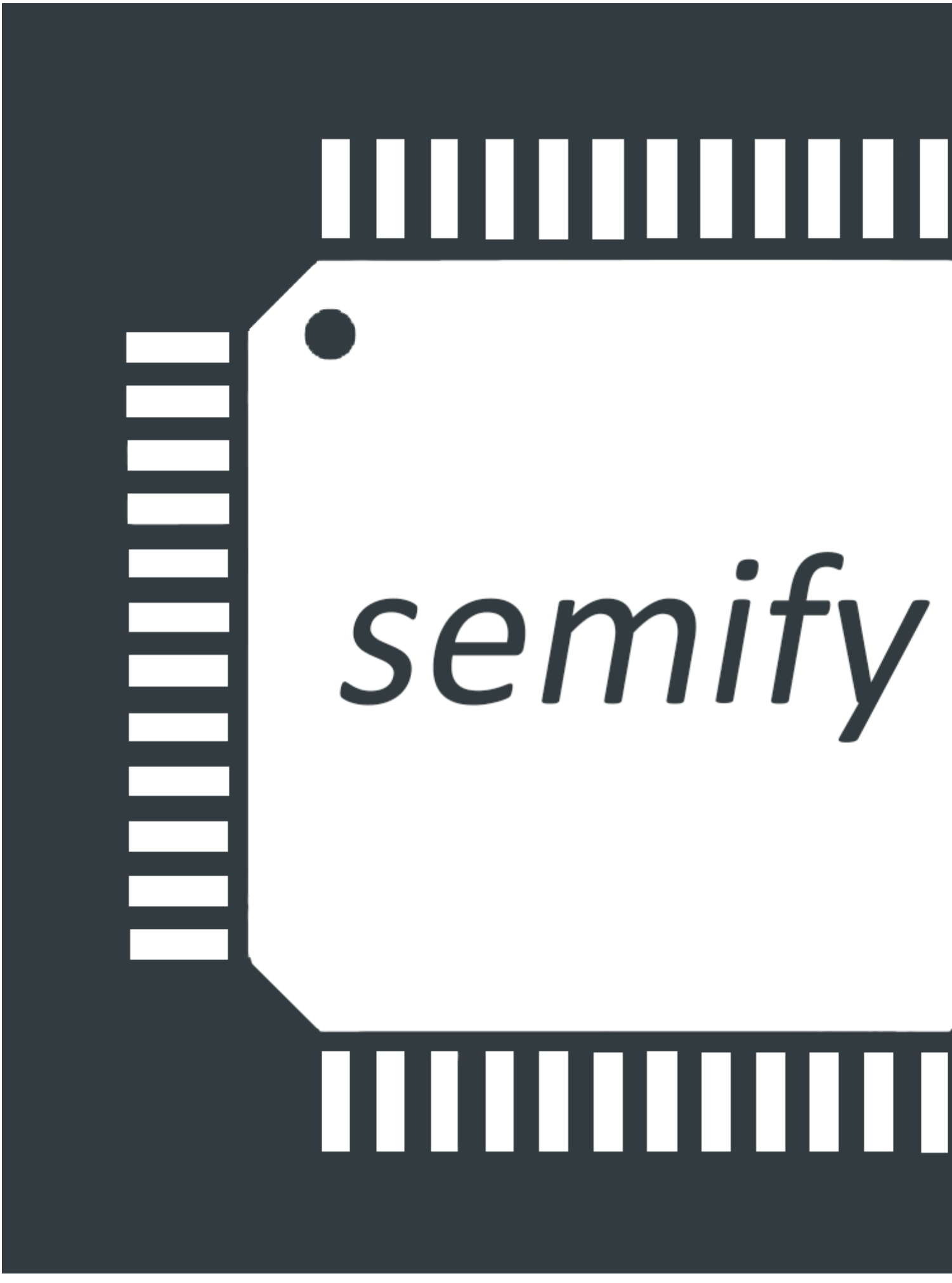
Science Park
The High Tech Incubator
Graz

AplusB
ACADEMIA PLUS


N131
G7B3


semify

semify

Ease the Life of Verification Engineers by helping them to analyze and understand failing simulation faster

Most of the functionality of today's semiconductor components consists of digital logic circuits. During the development process of these digital circuits for ASICs (Application Specific Circuit) as well as for FPGAs (Field Programmable Gate Array), verification consumes a very large portion of the overall development effort. Depending on the functionality of the semiconductor component, this portion can take up to 50% of the development effort.

A precise analysis of the verification effort reveals that debugging (analyzing errors that occur during verification) represents the largest part of the verification effort. Debugging is a task that is still associated with a very large proportion of manual engineering work. Automating this step offers a great potential for effort and cost reduction of the digital verification process.

This is exactly where the “ErrorAnalyzer” tool comes in. ErrorAnalyzer analyzes the error patterns that occur during the simulation of digital circuits and suggests the most likely error patterns to the verification engineer. Based on the suggested error patterns, it is then possible for the verification engineer to quickly and efficiently find out the root cause of the underlying error. For the analysis, it is irrelevant whether the error occurred during the implementation of the digital circuit or inside the verification environment.

The analysis of the error pattern is a step during the verification process which has been carried out manually up to now. For this reason, the use of the ErrorAnalyzer achieves a significant increase in productivity when verifying digital circuits.

Team semify

Contact: Office (office@semify-eda.com)

Website: https://www.semify-eda.com